# PORT BYPASS AND REPEATER FOR FIBRE CHANNEL ARBITRATED LOOP S2058

## FEATURES

- ANSI X3T11 Fibre Channel Compatible
- Monolithic Clock Recovery Unit
  - Re-times & Buffers Received Data
  - Jitter Peaking < 0.15 dB
- Lock Detect Function
  - Run Length Violation Detector
  - Frequency Detection
- Port Bypass Circuit
- Suitable for both Coaxial and Optical Link

## APPLICATIONS

- Low Power Operation 0.425W, Typical
- 106.25 or 53.125 MHz Reference Clock
- 28-Pin SOIC Package
- 3.3V Supply

## GENERAL DESCRIPTION

The Fibre Channel Port Bypass with Repeater Circuit is used in full-speed (1.0625 Gb/s) Disk Arrays. The S2058 block diagram is shown in Figure 1. It contains a monolithic Clock Recovery Unit (CRU), a lock detect feature and a port bypass Circuit. The CRU may be used alone to implement a general purpose Repeater needed for many Disk Array and Switch applications where a re-timed and buffered signal is required. The S2058 may be used to implement a single chip Arbitrated Loop Port Bypass Retiming Node. The S2058 performs the function of a port bypass circuit followed by a clock and data retiming Phase Locked Loop (CDR). The CDR retimes incoming serial data, detects whether a valid signal is present and outputs a low jitter serial data stream.

## FUNCTIONAL DESCRIPTION

The S2058 performs two functions. The first is a Port Bypass Circuit (PBC) for nodes in a FC-AL system. The low jitter accumulation of the Port Bypass Path is essential in these systems. The second function is to retime and restore signal quality in RAID drives using the FC-AL link configuration. The low jitter transfer peaking and the high jitter tolerance specifications of the Clock and Data Recovery PLL are essential in these applications. In addition, the Lock detect circuit monitors the incoming signals for valid 8B/10B run length, transition density and frequency. The output of this circuit is useful for link performance monitoring and detection of channel present.

### Jitter Performance

The S2058 complies with the minimum jitter tolerance requirements proposed by the Fibre Channel jitter working group when used with differential inputs and outputs as shown in Figure 2. In addition, the S2058 is designed for minimum jitter generation and jitter transfer specifications. This allows the optimum system design for arbitrated loop architectures.

### Jitter Tolerance

Input jitter tolerance is defined as the amplitude of frequency dependent, random and deterministic jitter that causes the clock recovery PLL to violate the BER specifications. Input jitter tolerance specifications are shown in Figures 3 and 4.

***Figure 1. S2058 Block Diagram***

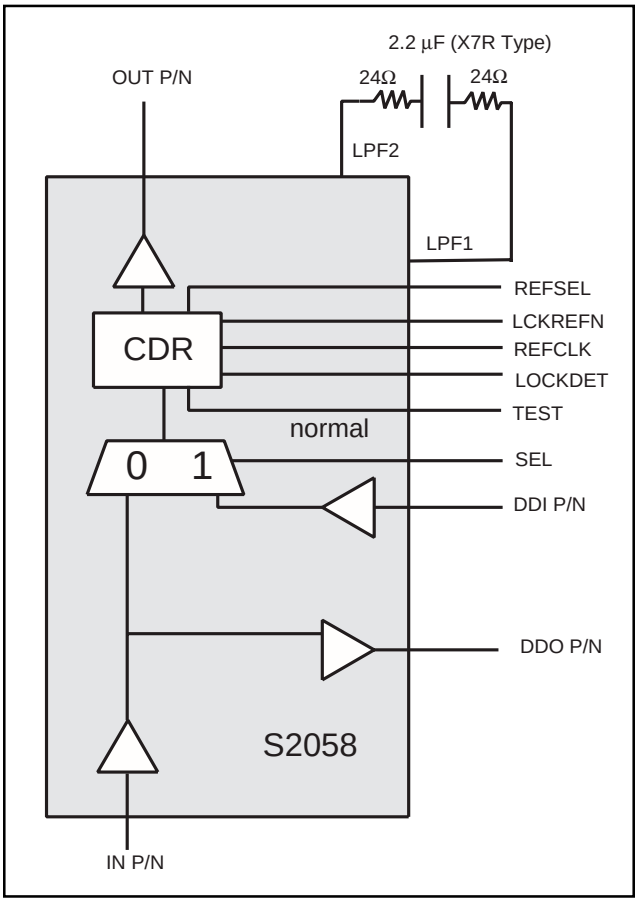
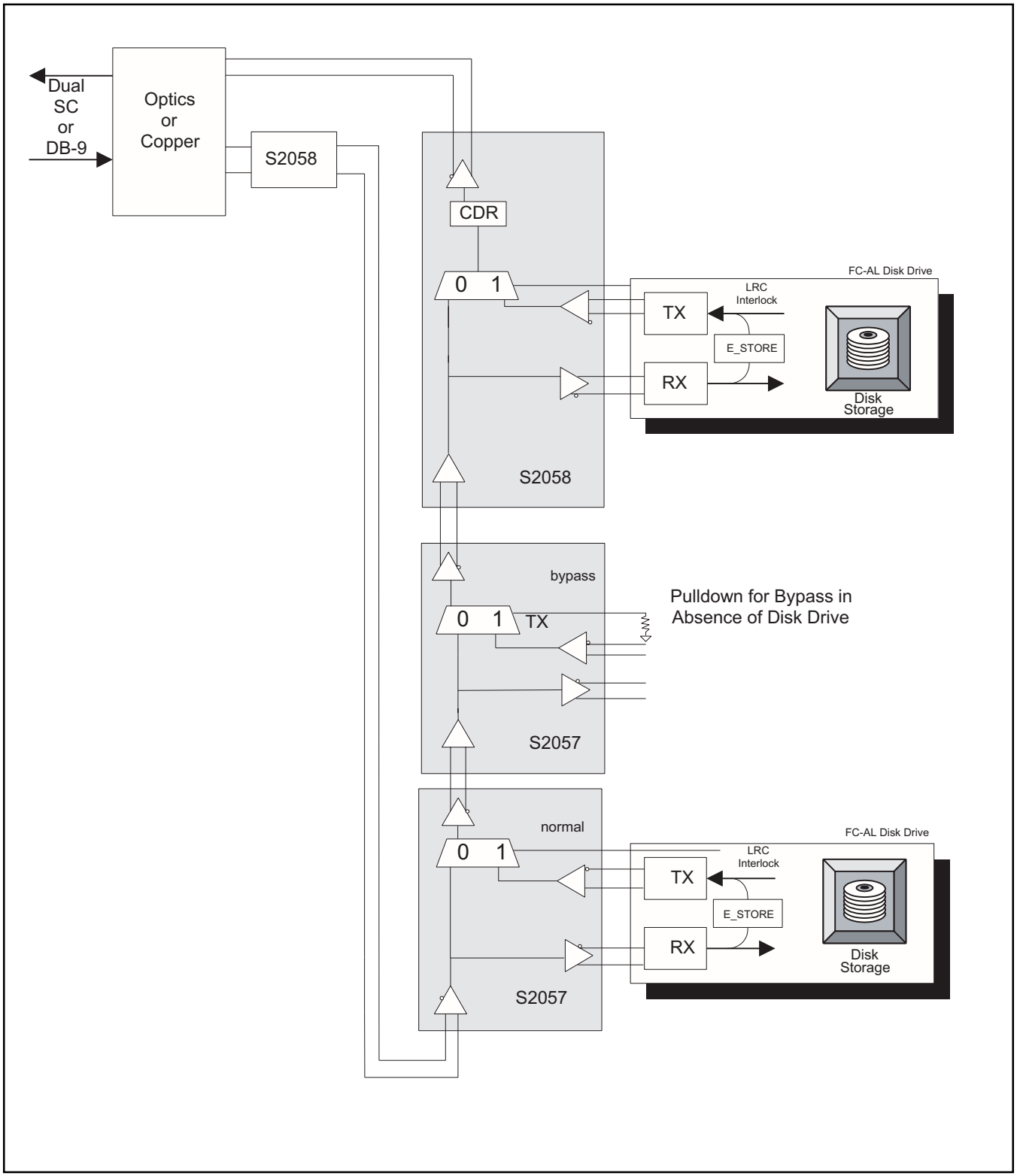


***Figure 2. FC-AL JBOD Application for Repeaters***



## FREQUENCY DEPENDENT JITTER TOLERANCE

Frequency Dependent Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal. See Figure 3.

**Random Jitter Tolerance**

Random Jitter Tolerance is the amount of jitter with a gaussian distribution that the clock recovery PLL must tolerate.

**Deterministic Jitter Tolerance**

Deterministic Jitter Tolerance is the amount of Deterministic jitter that the clock recovery PLL must tolerate.

## JITTER TRANSFER

Jitter transfer is defined as the ratio of jitter on the output signal to the jitter applied on the input signal versus frequency. Jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 is applied and the output jitter is measured for compliance to the mask of Figure 5. The jitter transfer mask includes specifications for both jitter peaking and bandwidth.

## LOCK DETECT

The S2058 lock detect circuit monitors the selected input signal to detect the presence of the channel. This is done by monitoring the run length, transition density and frequency content of the incoming data. The frequency monitor circuit checks the difference between the divided down recovered clock and the externally supplied reference clock (REFCLK). If the frequency difference of the recovered clock and the reference clock varies by more than +/- 240 ppm the part will be declared out of lock. In the out of lock state the PLL will lock to the local reference clock and periodically poll the serial data input looking for data with valid frequency content. In this state the LOCKDET output will shift between high and low states, mirroring the PLL as it locks to REFCLK (LOCKDET INACTIVE) and input data (LOCKDET ACTIVE).

***Figure 3. Input Jitter Tolerance***

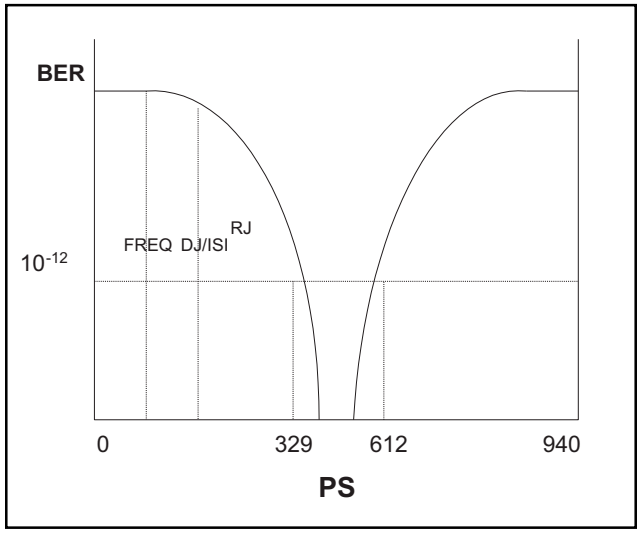



***Figure 4. Frequency Dependent Jitter Tolerance Mask***

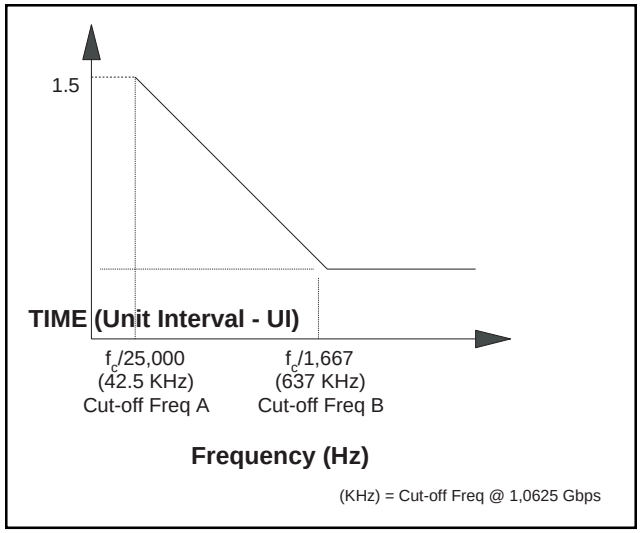



***Figure 5. Jitter Transfer Specification***

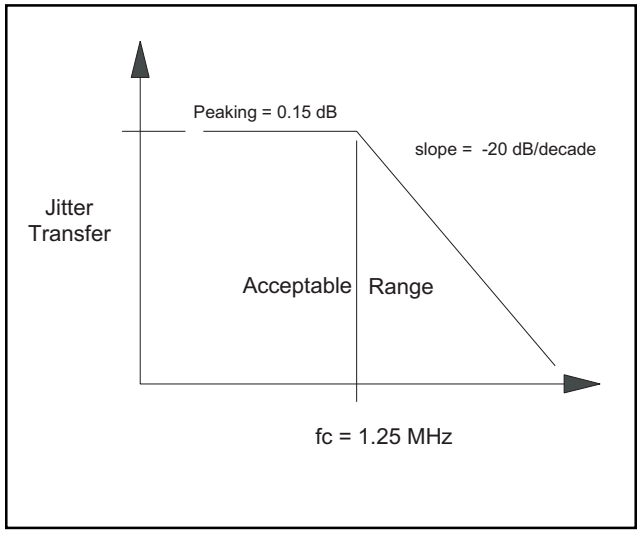
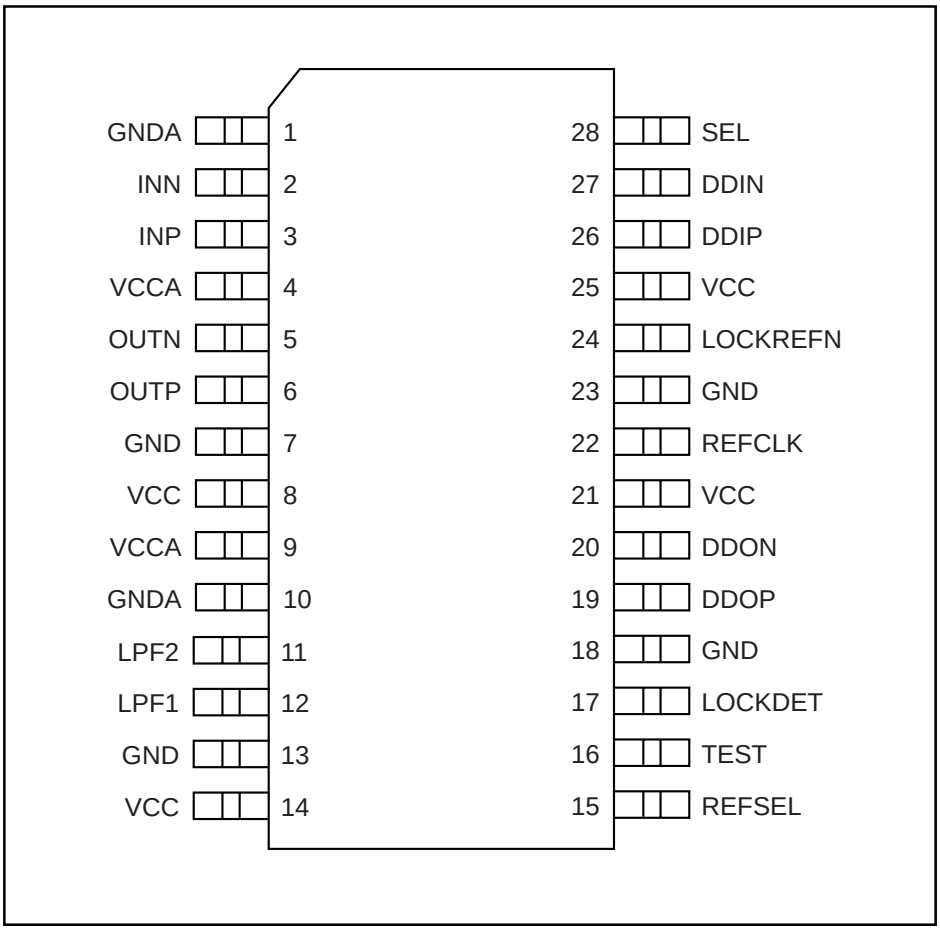


***Table 1. Pin Description***

| Pin Name | Level | I/O | Pin# | Description |
|---|---|---|---|---|
| OUTP<br>OUTN | Diff.<br>LVPECL | O | 6, 5 | Serial output to be connected to the next PBC in the loop. (See Figure 2.) This output has been retimed by the clock and data recovery PLL. |
| INN<br>INP | Diff.<br>LVPECL | I | 2, 3 | Serial input from the previous Port Bypass Circuit. |
| DDIP<br>DDIN | Diff.<br>LVPECL | I | 26, 27 | Serial input to the port bypass. This input should be driven by the FC-AL disk drive connected to the port bypass. This input is routed to the CDR block if the port bypass is in Normal operating mode. |
| REFCLK | TTL | I | 22 | Reference clock for the PLL, nominally at 106.25 MHz, rising edge active. |
| LPF1<br>LPF2 | Analog | | 12, 11 | Loop filter capacitor pins |
| LCKREFN | 3 State<br>TTL | I | 24 | Active Low. When inactive, the CDR PLL will attempt to lock to input data (normal operation). When active, the CDR PLL will be forced to lock to the local reference clock (REFCLK). When disconnected, the S2058 will be put into test mode and the PLL will be bypassed for factory testing. |
| LOCKDET | TTL | O | 17 | Active High. When active, LOCKDET indicates the CDR PLL is locked to the serial data stream. When inactive, the CDR PLL is locked to the local reference clock indicating a loss of data condition. (See Lock Detect section.) |
| DDON<br>DDOP | LVPECL | O | 20, 19 | Port bypass output. This output should drive the input port of the FC-AL disk drive. |
| SEL | TTL | I | 28 | Port bypass B bypass control. When SELB is Low, the port bypass will be in bypass mode. When SEL is High, port bypass will be in normal mode. |
| GND | Ground | | 7, 13,<br>18, 23 | Ground pins are physically mounted to the die surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible. |
| VCC | | | 8, 14, 21,<br>25 | +3.3V Power supply. |
| VCCA | Analog | | 4, 9 | +3.3V Power supply for the CRU. |
| GNDA | Analog | | 1, 10 | Ground for the CRU |
| TEST | 3 Level<br>TTL | I | 16 | Used for manufacturing test. Normal chip operation when held Low. |
| REFSEL | TTL | I | 15 | Active Low. When active allows 106.25 MHz reference clock. When inactive, allows 53.125 MHz clock. |

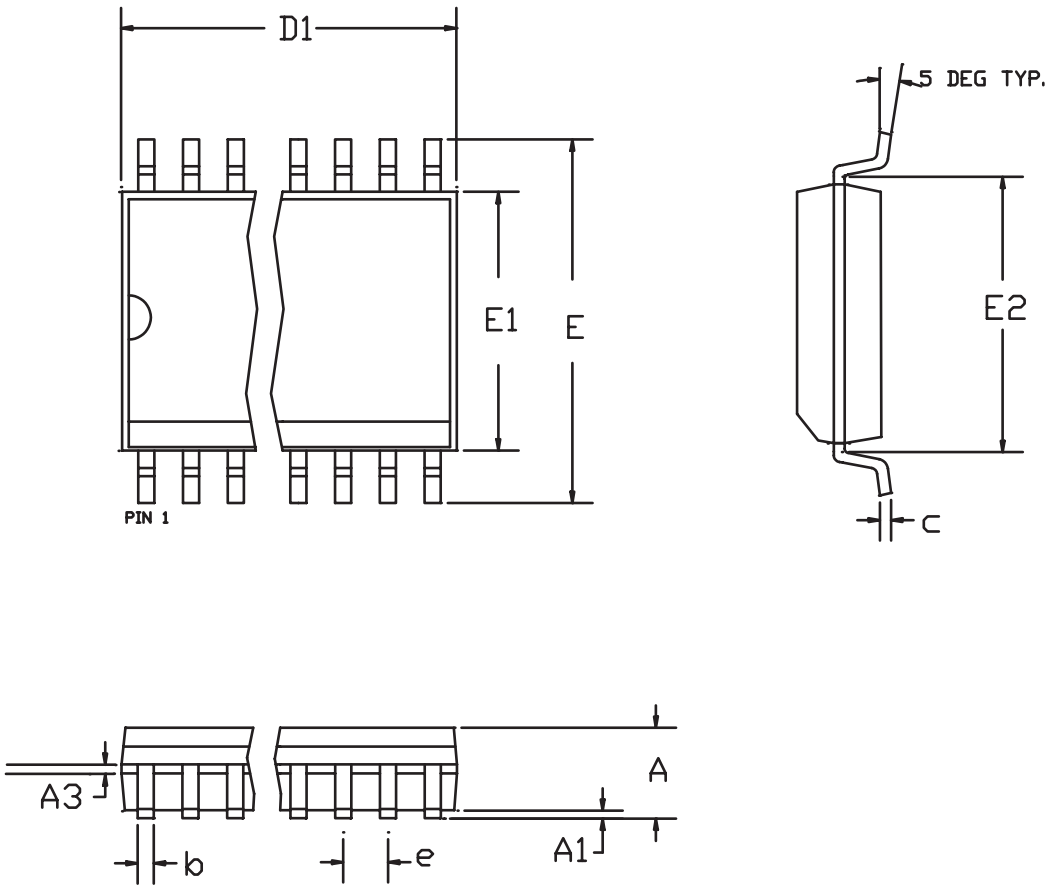
***Figure 6. S2058 Pinout Package***




***Thermal Information***

| Device | Θja (Still Air) |
|---|---|
| S2058 | 53 ˚ C/W |

*Figure 7. S2058 28-SOIC Package*




DIMENSIONS (are in inches)

| UNIT | A | $A_1$ | $A_3$ | $D_1$ | E | $E_1$ | $E_2$ | e | b | c |
|---|---|---|---|---|---|---|---|---|---|---|
| MIN | .098 | .005 | | .699 | .396 | .291 | .318 | .050 BASIC | .018 BASIC | .007 |
| NOM | .101 | .008 | .010 | .704 | .406 | .294 | .328 | | | .008 |
| MAX | .104 | .011 | | .709 | .416 | .297 | .338 | | | .009 |

Note: Lead tip coplanarity after form to be within .004

***Table 2. AC Characteristics***

| Parameter | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_R$, $T_F$ | REFCLK rise and fall time | | 3.0 | ns | 10% to 90% |
| FT | REFCLK frequency tolerance | | 100 | ppm | Difference between REFCLK and RX data frequency. |
| DC | REFCLK duty cycle | 40/60 | | % | |
| **Jitter Specifications** | | | | | |
| RJOUT | Random Jitter (RMS) OUT P/N | | 20 | ps | RMS, tested on a sample basis. |
| DJOUT | Deterministic Jitter (p-p) OUT P/N | | 50 | ps | Peak-to Peak, tested on a sample basis. |
| FREQJT | Frequency dependent jitter tolerance IN P/N | 0.1 | | UI | Jitter tolerance mask per Fibre Channel Jitter specification. |
| RANJT | Random jitter tolerance IN P/N | | 0.22 | UI | Peak-toPeak |
| DJT | Deterministic jitter tolerance IN P/N | | 0.38 | UI | Peak-to-Peak @ >53.125 MHz |
| JXFR (Input to Output) | Jitter transfer peaking from IN P/N to OUT P/N | | 0.15 | dB | 1010 pattern |
| $t_{SR}$ $t_{SF}$ | DDO & DOUT | | 250 | ps | 20 to 80% |

***Table 3. LVTTL DC Characteristics***

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage (TTL) | 2.2 | | | V | $I_{OH}$ = -.1 mA |
| $V_{OL}$ | Output Low Voltage (TTL) | | | 0.5 | V | $I_{OL}$ = +1.2 mA |
| $V_{IH}$ | Input High Voltage (TTL) | 2.0 | | | V | |
| $V_{IL}$ | Input Low Voltage (TTL) | | | 0.8 | V | |
| $I_{IH}$ | Input High Current (TTL) | | | 50 | µA | $V_{IN}$ = 2.4V |
| $I_{IL}$ | Input Low Current (TTL) | -500 | | -50 | µA | $V_{IN}$ = 0.5V |
| $\Delta V_{OUT}$ | LVPECL Output differential peak-to-peak voltage swing | 1200 | | 2200 | mVp-p | 50? to $V_{CC}$ -2.0V |
| $\Delta V_{IN}$ | Receiver differential peak-to-peak input sensitivity, RX and SI | 200 | | 2600 | mVp-p | $V_{CC}$ = 3.3V, AC coupled. Internally DC biased to $V_{CC}$ -0.65V |

***Table 4. LVPECL Input/Output DC Characteristics***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{CC}$ -1.11 | $V_{CC}$ -0.67 | V | |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ -2 | $V_{CC}$ -1.3 | V | |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ -0.7 | $V_{CC}$ -0.2 | V | AC Coupled |
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ -0.7 | $V_{CC}$ -0.2 | V | AC Coupled |
| $V_{IH}$ | Input High Current | -250 | 200 | µA | |
| $V_{IL}$ | Input Low Current | -200 | 200 | µA | |

***Table 5. Absolute Maximum Ratings[1]***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| TTL Power Supply Voltage ($V_{CC}$) | 0.5 | | +4 | V |
| PECL DC Input Voltage ($V_{INP}$) | -0.5 | | $V_{CC}$+0.5 | V |
| TTL DC Input Voltage ($V_{INP}$) | -0.5 | | 5.5 | V |
| DC Voltage applied to outputs for High output state ($V_{IN\ TTL}$) | -0.5 | | $V_{CC}$+0.5 | V |
| TTL Output Current ($I_{OUT}$) (DC, Output High) | | | 50 | mA |
| PECL Output Current ($I_{OUT}$) (DC, Output High) | | | 50 | mA |
| Case Temperature Under Bias ($T_C$) | -55 | | 125 | ˚C |
| Storage Temperature ($T_{STG}$) | -65 | | 150 | ˚C |
| Maximum Input | 400 | 1K | 1500 | V |

1. CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

***Table 6. Recommended Operating Conditions [2]***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Power Supply Voltage ($V_{DD}$) | +3.1 | | +3.5 | V |
| Ambient Operating Temperature Range (T) | 0 | | 70 | ˚C |
| ICC Current Supply | | 125 | 200 | mA |

2. AMCC guarantees the functional and parametric operation of the part under "Recommended Operating Conditions," except where specifically noted in the AC and DC Parametric Tables.

***Figure 8. Output Circuit***

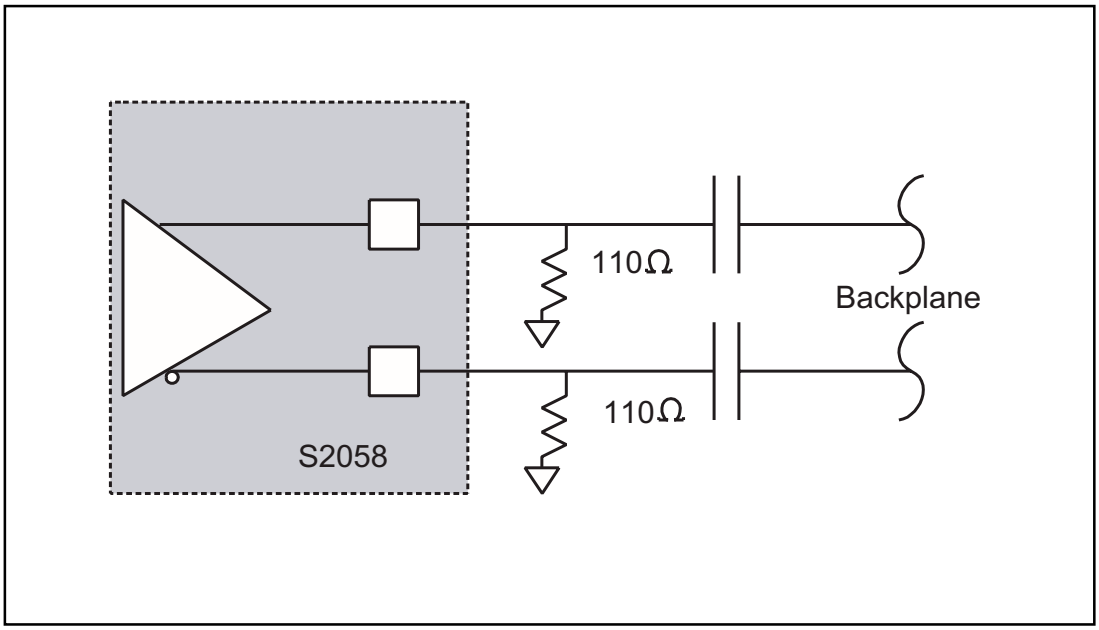
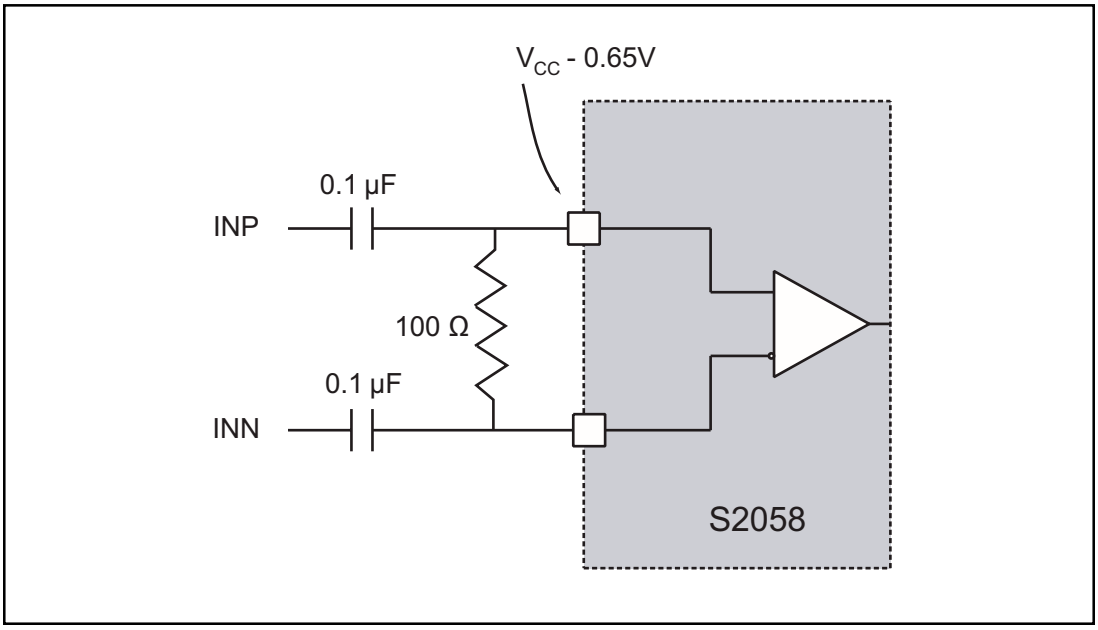



***Figure 9. High Speed Differential Inputs (L_Sin/IN)***



***Ordering Information***

| Grade | Device | Package |
|---|---|---|
| S – Commercial/ Industrial | 2058 | A – 28-Pin SOIC |

**X – XXXX – X**
Grade Part Number Package

ISO 9001 CERTIFIED

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